100GBASE-LR4 & OTU4 10km CFP2 Optical Transceiver

GF2-S101-LR4C

Features

- ✓ Hot-pluggable CFP2 form factor
- ✓ 4 channels full-duplex transceiver module
- ✓ Supports 111.8Gb/s aggregate bit rate
- ✓ 4 channels DFB LAN-WDM cooling transmitter
- ✓ 4 channels PIN ROSA
- ✓ TX input and RX output CDR retiming
- ✓ 6W maximum power dissipation
- ✓ Maximum link length of 10km on SMF
- ✓ Duplex LC receptacle
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature range: 0 to 70°C
- ✓ Single 3.3V power supply
- ✓ RoHS-6 compliant (lead free)

Applications

- ✓ 100GBASE-LR4 100G Ethernet
- ✓ OTN OTU4 applications

Description

The Gigalight 100GBASE-LR4 & OTU4 10km CFP2 optical transceiver, 100G CFP2 LR4/OTU4 (GF2-S101-LR4C) is designed for use in 100-Gigabit Ethernet and OTN links up to 10km on Single Mode Fiber (SMF). It is compliant with the CFP2 MSA, IEEE 802.3ba 100GBASE-LR4, and OTU4 standards. Digital diagnostics functions are available via an MDIO interface, as specified by the CFP2 MSA. It integrates the transmit and receive path onto one module. On the transmit side, four lanes of serial data streams are recovered, retimed, and passed on to four laser drivers, which control four DFB lasers with LAN-WDM 1295.56nm, 1300.05nm, 1304.58nm, and 1309.14nm center wavelengths. The optical signals are then multiplexed into a single-mode fiber through an industry-standard LC connector. On the receive side, four lanes of optical

data streams are optically demultiplexed by an integrated optical demultiplexer. Each data steam is recovered by a PIN photodetector and transimpedance amplifier, retimed, and passed on to an output driver. This module features a hot-pluggable electrical interface, low power consumption, and MDIO management interface.

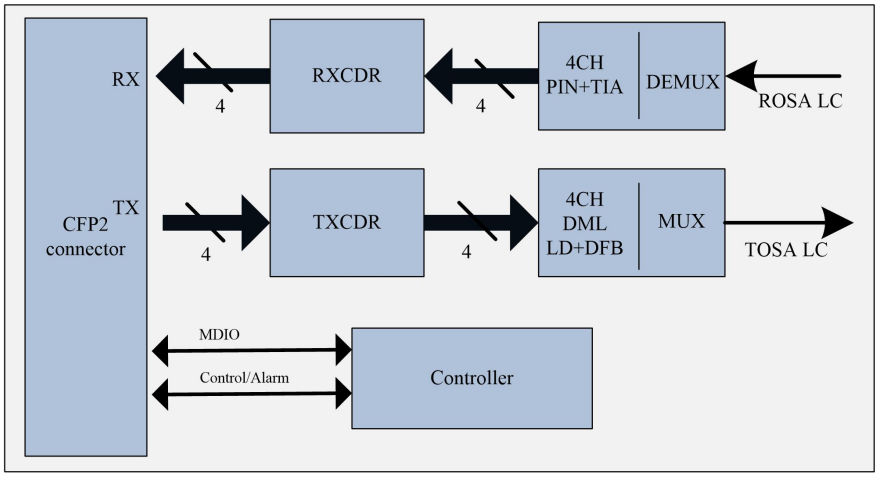


Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.5	3.6	V
Input Voltage	V_{in}	-0.3	V_{cc}+0.3	V
Storage Temperature	T_s	-40	85	ºC
Case Operating Temperature	T_c	0	70	ºC
Humidity (non-condensing)	Rh	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Supply Current	I_{cc}			1.9	A
Operating Case Temperature	T_c	0		70	ºC
Data Rate Per Lane	fd		25.78125	27.95	Gb/s
Humidity	Rh	5		85	%
Power Dissipation	P_m			6	W
Aggregate Bit Rate	BR_{aggr}		103.125	111.8	Gb/s

Optical Characteristics

Parameter	Symbol	Unit	Min	Typical	Max
Optical Transmitter Characteristics (each lane)					
Signaling Rate (100GbE)		Gb/s		25.78125	
Signaling Rate (OTU4)				27.9525	
Four Lane Wavelength Range	λ1	nm	1294.53	1295.56	1296.59
	λ2		1299.02	1300.05	1301.09
	λ3		1303.54	1304.58	1305.63
	λ4		1308.09	1309.14	1310.19
Side Mode Suppression Ratio	SMSR	dB	30		
Total Average Launch Power	P_t	dBm			10.5
Average Launch Power (100GbE)	P_a	dBm	-4.3		4.5
Average Launch Power (OTU4)			-0.6		4.5
OMA[1]	P_{OMA}	dB	-1.3		4.5
Extinction Ratio	ER	dB	4		
Average Launch Power OFF	P_{off}	dBm			-30
Optical Receiver Characteristics (each lane)					
Receiver Sensitivity in OMA[2] (100GbE)	S_{OMA}	dBm			-8.6
Receiver Sensitivity[2] (OTU4)					-8.4
Los Assert	LOS_A	dBm	-18		-14
Los De-assert	LOS_D	dBm			-13
Los Hysteresis	LOS_H	dBm		0.5	
Damage Threshold[3]	TH_d	dBm	5.5		
Receive Power in OMA	P_{in_OMA}	dBm			4.5
Difference in Receive Power between any Two Lanes (OMA)	$P_{rx,diff}$	dB			5.5
Average Receive Power (100GbE)	P_{in}	dBm	-10.6		4.5
Average Receive Power (OTU4)			-6.9		4.5

Note:

1. Even if the TDP < 1dB, the OMA min must exceed the minimum value specified here.

2. Measured with conformance test signal at receiver input for BER=$1x10^{-12}$.

3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

Electrical Specifications

Parameter	Symbol	Unit	Min	Typical	Max	Note
Differential Data Output Swing	$V_{out,pp}$	mV	400		850	
Differential Input Voltage Swing	$V_{in,pp}$	mV			900	
Differential Signal Output Resistance		Ω	90		110	
Differential Signal Input Resistance		Ω	90		110	

Low Speed Electrical Interface

Parameter	Symbol	Unit	Min	Max	Note
Input Voltage	V_{IH}	V	2.0	V_{cc3}+0.3	
	V_{IL}	V	-0.3	0.8	
Output Voltage	V_{OH}	V	V_{dd3}-0.5	V_{dd3}+0.3	1
	V_{OL}	V	0.0	0.4	
Input Leakage Current	$3.3V_{IL}$	uA	-10	10	
Minimum Pulse Width of Control Pin Signal	T_CNTL	us	100		
1.2V LVCMOS Electrical Characteristics					
Input High Voltage	$1.2V_{IH}$	V	0.84	1.5	
Input Low Voltage	$1.2V_{IL}$	V	-0.3	0.36	
Input Leakage Current	$1.2I_{IN}$	uA	-100	100	
Output High Voltage	$1.2V_{OH}$	V	1.0	1.5	
Output Low Voltage	$1.2V_{OL}$	V	-0.3	0.2	
Output High Current	$1.2I_{OH}$	mA		-4	
Output Low Current	$1.2I_{OL}$	mA	4		
Input Capacitance	C_i	pF		10	

Note:

1. V_{dd3} is host +3.3V power supply.

Hardware Control Pins

The CFP2 module supports real-time control functions via hardware pins.

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
17	PRG_CNTL1	Programmable Control 1 MSA Default: TRXIC_RSTn , TX&RX ICs reset, "0": reset; "1"	I	3.3V LVCMOS	per CFP MSA Management Interface Specification		Pull-Up[1]
18	PRG_CNTL2	Programmable Control 2 MSA Default: Hardware Interlock LSB	I	3.3V LVCMOS			Pull-Up[1]
19	PRG_CNTL3	Programmable Control 3 MSA Default: Hardware Interlock MSB	I	3.3V LVCMOS			Pull-Up[1]
26	M0D_L0PWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up[1]
28	M0D_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down[2]
24	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up[1]

Note:

4. Pull-Up resistor (4.7K to 10K Ohm) is located within the CFP2 module.
5. Pull-Down resistor (4.7K to 10K Ohm) is located within the CFP2 module.

Hardware Alarm Pins

The CFP module supports alarm hardware pins.

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
20	PRG_ALRM1	Programmable Alarm 1 MSA Default: HIPWR_0N	O	3.3V LVCMOS			
21	PRG_ALRM3	Programmable Alarm 3 MSA Default: MOD_FAULT	O	3.3V LVCMOS			
22	MOD_ABS	Module Absent	O	3.3V LVCMOS			
27	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Absent	Present	Pull-Down[1]
25	PRG_ALRM3	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note:

1. Pull-Down resistor (<100ohm) is located within the CFP2 module. Pull-up should be located on the host.

Management Interface Pins (MDIO)

The CFP2 module supports alarm, control and monitor functions via an MDIO bus.

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
29	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
32	MDIO	Management Data Input Output Bi-Directional Data	I/0	1.2V LVCMOS			
31	MDC	MDIO Clock	I	1.2V LVCMOS			
33	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
34	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
35	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific May depend on current state Condition when signal is applied. See Vendor Datasheet

Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			ms	Value is dependent upon module start-up time. Please See register "Maximum High-Power-up ime" in "CFP MSA Management Interface Specification"
Receiver Loss of Signal Assert Time	t_loss_assert		100	us	Maximum value designed to support telecom applications
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	us	Maximum value designed to support telecom applications
Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	ms	This is a logical "OR" of Associated MDIO alarm& status registers. Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical "OR" of Associated MDIO alarm & status registers. Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific
Transmitter Enabled(TX_DIS_asserted)	t_assert		100	ms	Value is dependent upon module start-up time. Please See register "Maximum TX-Turn-on Time" in "CFP MSA Management Interface Specification"

Optional Transmitter and Receiver Monitor Clock Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency			3220		MHz	1/8 of Network lane rate
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

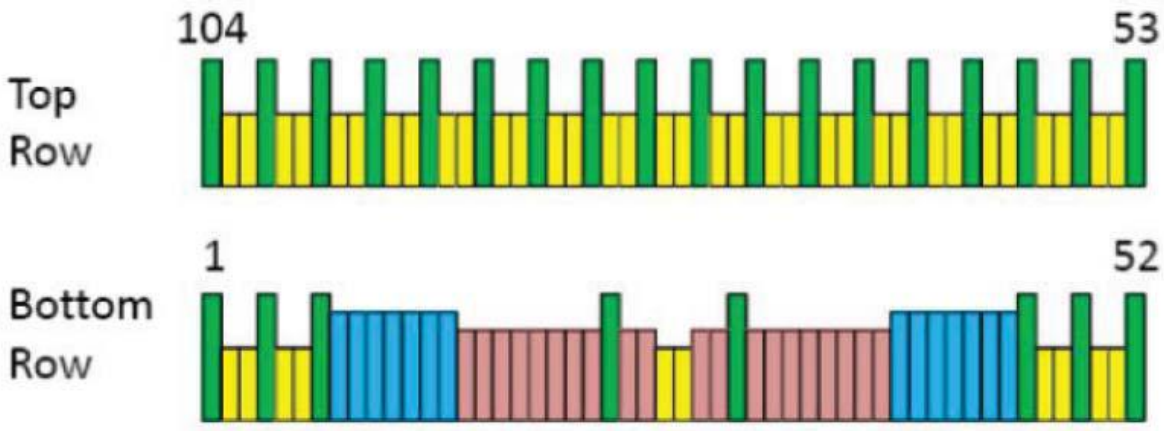
PIN Description

PIN#	Name	I/O	Logic	Description
1	GND			
2	(TX_MCLKn)	O	CML	For optical waveform testing. Not for normal use
3	(TX_MCLKp)	O	CML	For optical waveform testing. Not for normal use
4	GND			
5	N.C.			
6	N.C.			
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate, or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			

10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect!
16	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect!
17	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
18	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
19	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO
23	GND			
24	TX_DIS	I	LVCMOS	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0"= transmitter enabled
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O		Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 1
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 2
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 3
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 1

34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 2
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 3
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
46	3.3V_GND			
47	N.C.			
48	N.C.			
49	GND			
50	(RX_MCLKn)	O	CML	For optical waveform testing. Not for normal use.
51	(RX_MCLKp)	O	CML	For optical waveform testing. Not for normal use.
52	GND			
53	GND			
54	N.C.			
55	N.C.			
56	GND			
57	RX0p	O	CML	Output Data
58	RX0n	O	CML	Inverted Output Data
59	GND			
60	RX1p	O	CML	Output Data
61	RX1n	O	CML	Inverted Output Data
62	GND			
63	N.C.			
64	N.C.			
65	GND			
59	GND			
60	RX1p	O	CML	Output Data
61	RX1n	O	CML	Inverted Output Data
62	GND			
63	N.C.			
64	N.C.			
65	GND			
70	RX2n	O	CML	Inverted Output Data
71	GND			
72	RX3p	O	CML	Output Data
73	RX3n	O	CML	Inverted Output Data
74	GND			
75	N.C.			
76	N.C.			
77	GND			

78	NC			
79	NC			
80	GND			
81	N.C.			
82	N.C.			
83	GND			
84	TX0p	I	CML	Input Data
85	TX0n	I	CML	Inverted Input Data
86	GND			
87	TX1p	I	CML	Input Data
88	TX1n	I	CML	Inverted Input Data
89	GND			
90	N.C.			
91	N.C.			
92	GND			
93	N.C.			
94	N.C.			
95	GND			
96	TX2p	I	CML	Input Data
97	TX2n	I	CML	Inverted Input Data
98	GND			
99	TX3p	I	CML	Input Data
100	TX3n	I	CML	Inverted Input Data
101	GND			
102	N.C.			
103	N.C.			
104	GND			



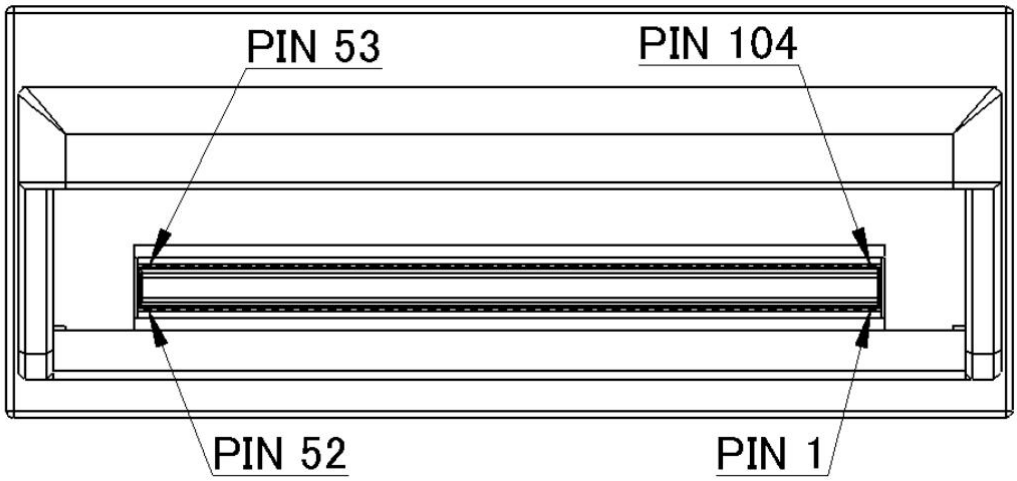
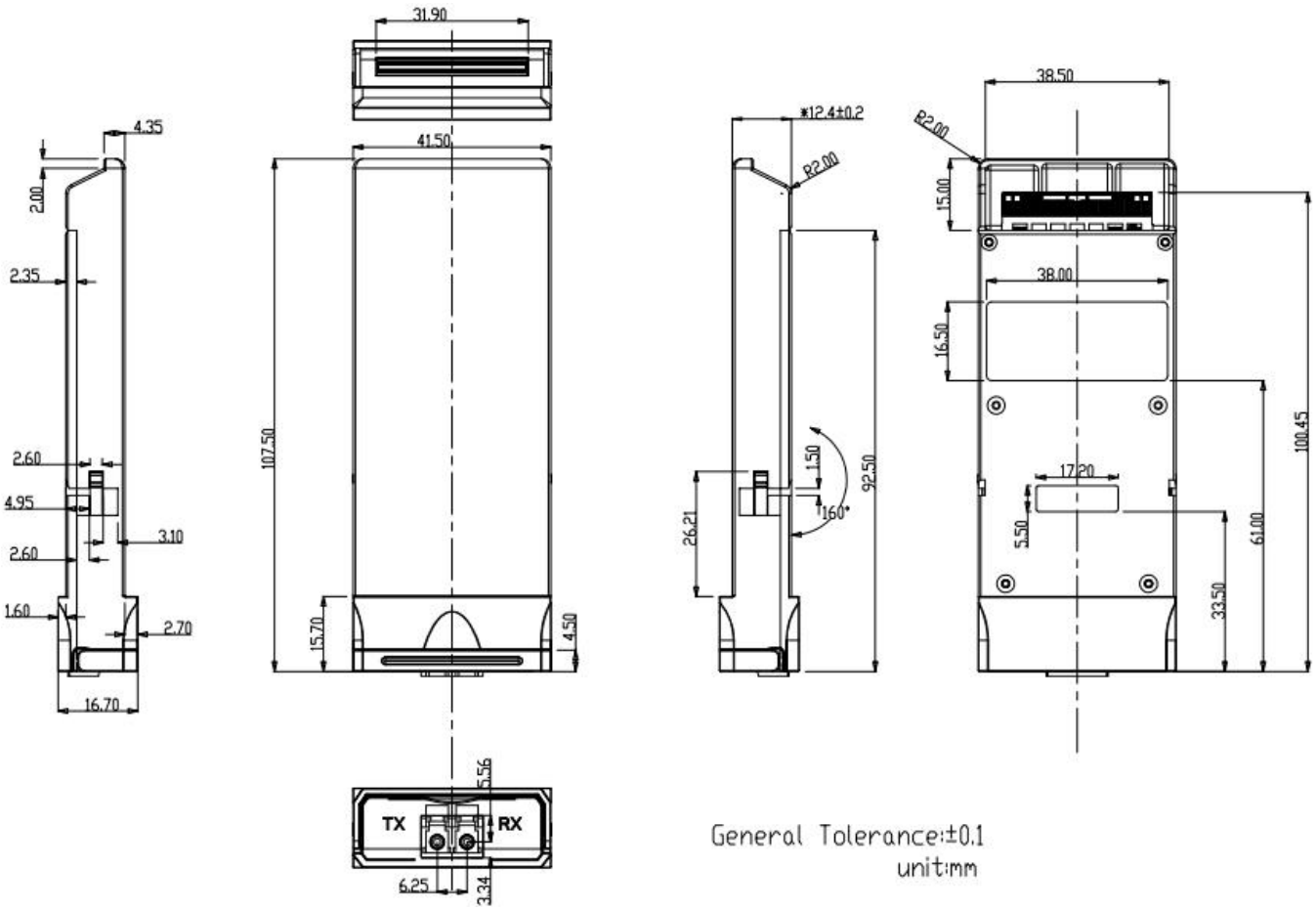


Figure 2. Pad Layout of the CFP2 Module

Mechanical Dimensions



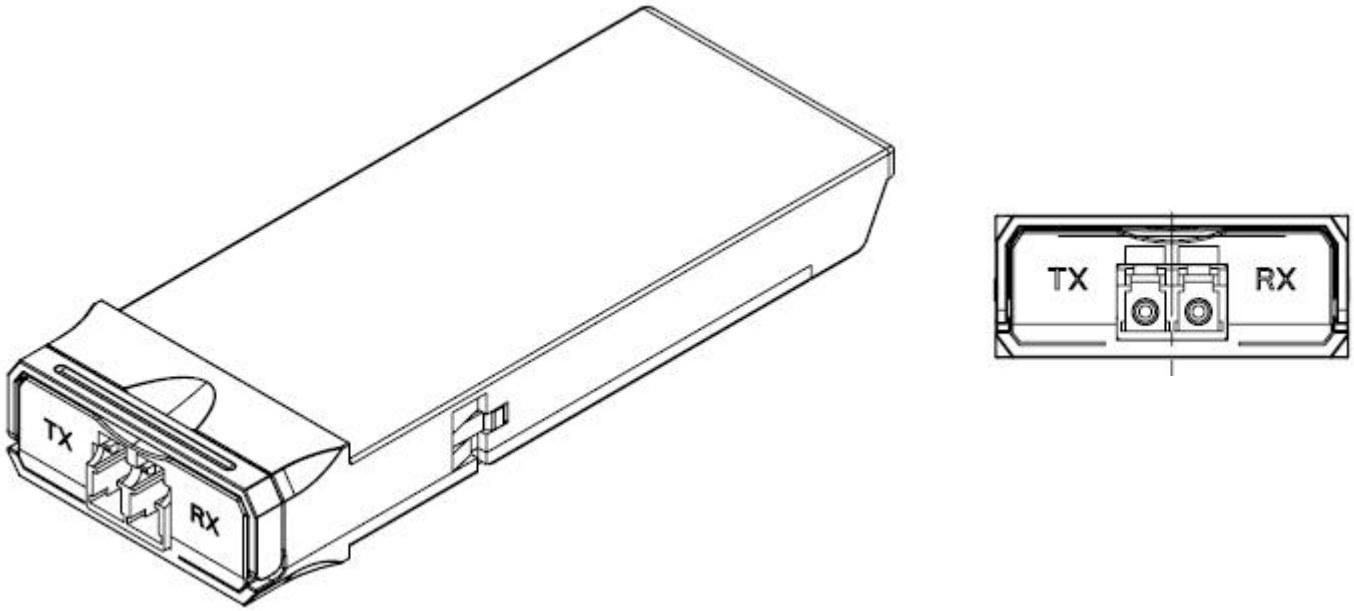


Figure 3. Mechanical Specifications

Ordering Information

Product Description	Part Number
CFP2 LR4, 111.8Gb/s, 1310nm, 10km, SMF, LC	GF2-S101-LR4C

References

1. CFP2 MSA
2. Ethernet 100GBASE-LR4
3. OTN OTU4

Regulatory Compliance

Feature	Test Method	Performance
Laser Eye Safety	FDA 21 CFR 1040.10 and 1040.11 IEC 60825-1: 1994+ A11: 1996+ A2: 2001 IEC 60825-2: 2004 + A1: 2006 EN 60825-1:1994+A1:2002+A2:2001 EN 60825-2: 2004	Compliant with Class 1 laser product
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7 Human Body Model	Class 1 (>1.5kV)
Electrostatic Discharge (ESD) Immunity	IEC 61000-4-2: 2001	Class 2 (>4.0kV)
Electromagnetic Interference (EMI)	FCC Part 15 Subpart J Class B CISPR22:1997+A1:2000+A2:2002, Class B EN55022:1998+A1:2000+A2:2003, Class B	Compliant with standards

Important Notice

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Revision History

Revision	Level	Date	Description
V0	Preliminary	Sep 2017	Advance Release.