100GBASE-LR4 & OTU4 10km CFP Optical Transceiver

GCF-S101-LR4C

Features

- ✓ Hot-pluggable CFP form factor
- ✓ 4 channels full-duplex transceiver module
- ✓ Supports 111.8Gb/s aggregate bit rate
- ✓ 4 channels DFB-based LAN-WDM cooling transmitter
- ✓ 4 channels PIN ROSA
- ✓ 9W maximum power dissipation
- ✓ Maximum link length of 10km on SMF
- ✓ Duplex LC receptacle
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature range: 0 to 70°C
- ✓ Single 3.3V power supply
- ✓ RoHS-6 compliant (lead free)

Applications

- ✓ 100GBASE-LR4 100G Ethernet
- ✓ OTN OTU4 applications

Description

The Gigalight 100GBASE-LR4 & OTU4 10km CFP optical transceiver, 100G CFP LR4/OTU4 (GCF-S101-LR4C) is designed for use in 100-Gigabit Ethernet and OTN links up to 10km on Single Mode Fiber (SMF). It is compliant with the CFP MSA, IEEE 802.3ba 100GBASE-LR4, and OTU4 standards. Digital diagnostics functions are available via an MDIO interface, as specified by the CFP MSA. The module converts 10-lane electrical data streams to 4-lane optical output signal and 4-lane optical input signal to 10-lane electrical data streams. This 10-lane electrical signal is fully compliant with 802.3ba CAUI specification and allows FR4 host PCB trace up to 25cm. The high-performance cooled LAN-WDM EML transmitter and high-sensitivity PIN receiver provide superior performance for 100-Gigabit Ethernet applications up to 10km links.

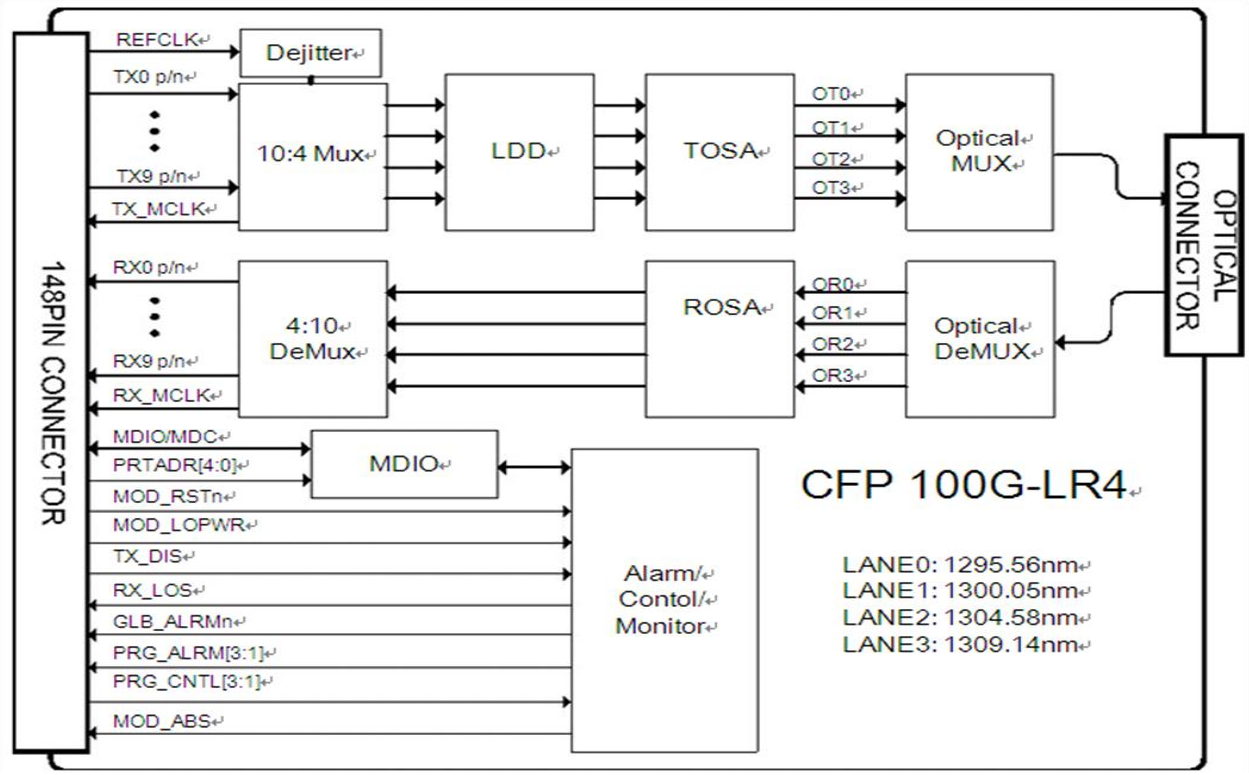

Figure 1: Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.5	3.6	V
Storage Temperature	T_s	-40	85	ºC
Case Operating Temperature	T_c	-5	75	ºC
Humidity (non-condensing)	Rh	5	85	%
Receiver Damage Threshold (each lane)	P_{dag}	5.5		dBm

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.2	3.3	3.4	V
Operating Case Temperature	T_c	0		70	ºC
Data Rate			103.125	111.8	Gb/s

Products Characteristics (tested under recommended operating conditions)

Parameter	Symbol	Unit	Min	Typical	Max	Notes
Voltage Supply Electrical Characteristics						
Supply Current Tx / Rx	I_{cc}	A			3	1
Power Supply Noise	V_{rip}				2%	DC-1MHz
					3%	1-10MHz
Dissipation Class2	P_w	W			9	
Low Power Dissipation	P_{low}	W			2	
Inrush Current n 2	I_{inrush}	mA/usec			50	
Turn-off Current Class2	$I_{turnoff}$	mA/usec	-50			
Different Signal Electrical Characteristics						
Single Ended Data Input Swing		mV	55		525	
Single Ended Data Output Swing		mV	180		385	
Differential Signal Resistance	Output	Ω	80		120	
Differential Signal Resistance	Input	Ω	80		120	
3.3V LVCMOS Electrical Characteristics						
Input High Voltage	$3.3V_{IH}$	V	2.0		Vcc+0.3	
Input Low Voltage	$3.3V_{IL}$	V	-0.3		0.8	
Input Leakage Current	$3.3I_{IN}$	uA	-10		10	
Output High Voltage	$3.3V_{OH}$	V	V_{cc}-0.2			I_{OH}=100uA
Output Low Voltage	$3.3V_{OL}$	V			0.2	I_{OL}=100uA
Pulse Width of Control Pin Signal	T_CNTL	us	100			
1.2V LVCMOS Electrical Characteristics						
Input High Voltage	$1.2V_{IH}$	V	0.84		1.5	
Input Low Voltage	$1.2V_{IL}$	V	-0.3		0.36	
Input Leakage Current	$1.2I_{IN}$	uA	-100		100	
Output High Voltage	$1.2V_{OH}$	V	1.0		1.5	
Output Low Voltage	$1.2V_{OL}$	V	-0.3		0.2	
Output High Current	$1.2I_{OH}$	mA			-4	
Output Low Current	$1.2I_{OL}$	mA	4			
Input Capacitance	C_i	pF			10	
Optical Transmitter Characteristics (each lane)						
Signaling Rate @100GbE		Gb/s		25.78125+/-100ppm		
Signaling Rate @OTU4				27.95249+/-20ppm		
Wavelength Range	λ1	nm	1294.53	1295.56	1296.59	
	λ2		1299.02	1300.05	1301.09	
	λ3		1303.54	1304.58	1305.63	
	λ4		1308.09	1309.14	1310.19	
Side Mode Suppression Ratio	SMSR	dB	30			
Total Average Launch Power	P_t	dBm			10.5	@100GbE
					8.9	@OTU4
Average Launch Power[2]	P_a	dBm	-4.3		4. 5	@100GbE
			-2.5		2.9	@OTU4
Optical Modulation Amplitude	OMA	dBm	-1.3		4.5	3

Transmitter and Dispersion Penalty	TDP	dB			2.2	@100GbE
					1.5	@OTU4
Average Launch Power of Off Transmitter	P_{off}	dBm			-30	
Extinction Ratio	ER	dB	4			@100GbE
			7			@OTU4
Channel Power Difference		dB			5	
RIN20 OMA		dB/Hz			-130	
Optical Return Loss Tolerance	T_{RL}	dB			20	
Transmitter Reflectance	R_T	dB			-12	4
Eye Diagram		Compliant with IEEE 802.3ba-2010/G.959.1)				
Optical Receiver Characteristics (each lane)						
Receive Rate		Gb/s		25.78125+/-100ppm		@100GbE
				27.95249+/-20ppm		@OTU4
Four Lane Wavelength Range	λ1	nm	1294.53	1295.56	1296.59	
	λ2		1299.02	1300.05	1301.09	
	λ3		1303.54	1304.58	1305.63	
	λ4		1308.09	1309.14	1310.19	
Overload Input Optical Power	P_{max}	dBm	4.5			5
Total Input Optical Power	P_t	dBm			8.9	@OTU4
Average Receive Power[6]	Pin	dBm	-10.6		4.5	@100GbE
			-8.8		2.9	@OTU4
Receive Power in OMA	P_{inOMA}	dBm			4.5	
Difference in Receive Power		dBm			5.5	
Receiver Sensitivity in OMA	Pmin	dBm			-8.6	@100GbE[7]
					-10.3	@OTU4[8]
Stressed Receiver Sensitivity in OMA[9, 10]		dBm			-6.8	
Los Assert	LOS_A	dBm	-20		-15	
Los De-assert	LOS_D	dBm			-14	
Los Hysteresis	LOS_H	dBm	0.5			
Chromatic Dispersion		Ps/nm	-28.5		+9.5	
Maximum Reflectance		dB			-26	
Delay Group Differential		ps			8	

Notes:

1. The supply current includes CFP module's supply current and test board working current.
2. Each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Even if the TDP < 1dB, the OMA (min) must exceed this value.
4. Defined looking into the transmitter.

5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
6. Each lane (max) for 100GBASE-ER4 is larger than the 100BASE-ER4 transmitter value to allow compatibility with 100BASE-LR4 units at short distances. Each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
7. Each lane (max) is informative.
8. Measured with PRBS 2^{31}-1 for BER=10^{-5}. The BER for the OTU4 application is required to be met only after FEC has been applied.
9. Measured with conformance test signal at TP3 for BER=10^{-12}
10. Conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB; stressed eye J2 jitter for each lane is 0.3UI; stressed eye J9 jitter for each lane is 0.47UI.

Hardware Control Pins

The CFP module supports real-time control functions via hardware pins.

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down[1, 2]
30	PRG_CNTL1	Programmable Control 1 MSADefault: TRXIC_RST n , TX&RX ICs reset, "0":reset; "1"	I	3.3V LVCMOS	per CFP MSA Management Interface Specification		Pull-Up
31	PRG_CNTL2	Programmable Control 2 MSA Default : Hardware Interlock LSB	I	3.3V LVCMOS			Pull-Up
32	PRG_CNTL3	Programmable Control 3 MSA Default: Hardware Interlock MSB	I	3.3V LVCMOS			Pull-Up
36	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up
37	MOD_LOPW R	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up
39	MOD_RSTn	Module Reset (Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down

Note:

1. Pull-Up resistor (4.7k to 10k Ohm) is located within the CFP module.
2. Push-Down resistor (4.7k to 10k Ohm) is located within the CFP module.

Hardware Alarm Pins

The CFP module supports alarm hardware pins.

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down[1, 2]
33	prg_alrm1	Programmable Alarm 1 MSA Default:HIPWR_ON	O	3.3V LVCMOS	Active High per MDIO document		
34	PRG ALRM 2	Programmable Alarm 2MSA default:MOD_READY , Ready State has been reached	O	3.3V LVCMOS			
35	PRG ALRM3	Programmable Alarm 3 MSA Default: MOD FAULT	O	3.3V LVCMOS			
38	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull-Down
40	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note:

1. Pull-Up resistor (4.7k to 10k Ohm) is located within the CFP module.
2. Push-Down resistor (4.7k to 10k Ohm) is located within the CFP module.

Management Interface Pins (MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus.

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
41	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Absent	Alarm	Pull-Down
47	MDIO	Management Data Input Output Bi-Directional Data	I/0	1.2V LVCMOS			
48	MDC	MDIO Clock	I	1.2V LVCMOS			
46	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
45	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
44	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			
43	PRTADR3	MDIO Physical Port address bit3	I	1.2V LVCMOS			
42	PRTADR4	MDIO Physical Port address bit4	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Parameter	Symbol	Min	Max	Unit	Notes& Conditions
Hardware MOD_LOPWR Assert	t_MOD_LOPWR_Assert		1	ms	Application specific may depend on current state condition when signal is applied.
TX Disable Assert Time	T_off		100	us	

Electrical Characteristics

Reference Clock Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Impedance	Z_d	80	100	120	Q	
Frequency			161.1328125/ 644.53125		MHz	1/64 or 1/16 of electrical lane rate
Frequency Stability	△f	-100		100	ppm	For Ethernet applications
		-20		20		For Telecom applications
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
RMS Jitter1-2	0			10	ps	Random Jitter Over frequency band of 10KHz<f<10MH
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	tr/f	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

Note:

1. The term "40GBASE_FR" is the 40GbE serial optical interface in the task force phase at IEEE-SA at the time of this publication. Also, 1/16 of optical lane clock is recommended for TX_MCLK and RX_MCLK.
2. Multi-protocol modules are recommended to adopt the clock rate rate used in Telecom applications.

Optional Transmitter and Receiver Monitor Clock Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes& Conditions
Impedance	Z_d	80	100	120	Q	
Frequency					MHz	1/8 of Network lane rate
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

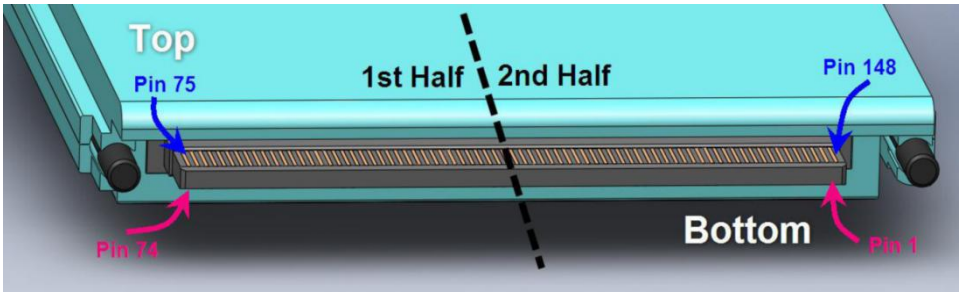

Figure 2. Pad Layout

Mechanical Dimensions

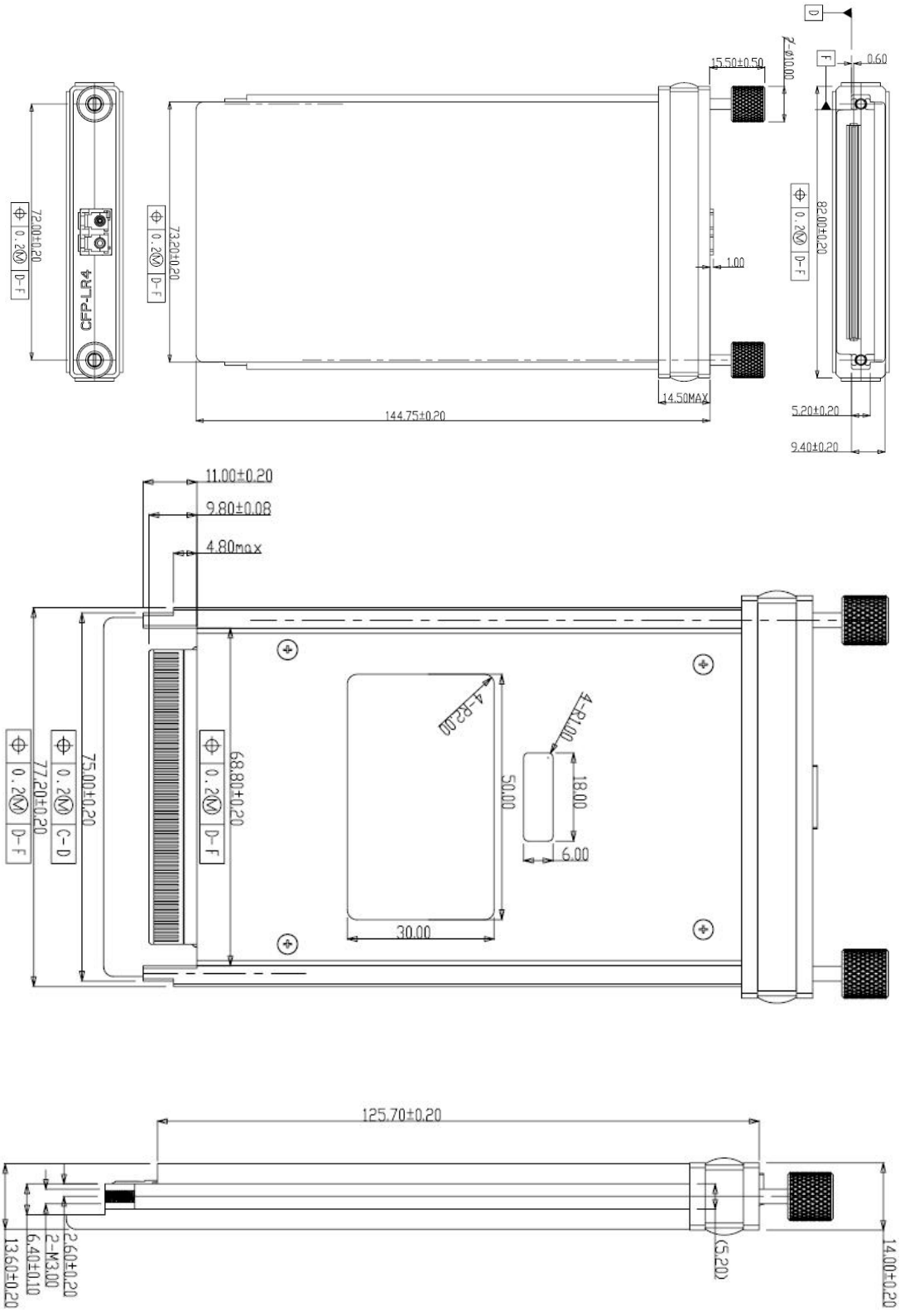

Figure 3. Mechanical Specifications

Ordering Information

Product Description	Part Number
CFP LR4, 111.8Gb/s, 1310nm, 10km, SMF, LC	GCF-S101-LR4C

References:

1. 100GBASE-LR4 100G Ethernet
2. OTN OTU4
3. CFP MSA

ESD:

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety:

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Important Notice:

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by GIGALIGHT before they become applicable to any particular order or contract. In accordance with the GIGALIGHT policy of continuous improvement specifications may change without notice.
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Revision History

Revision	Level	Date	Description
V0	Preliminary	Feb 2017	Advance Release.