

100GBASE-SR10 & OTU4 400m CFP2 Optical Transceiver GF2-M101-SR10C

Features

- ✓ Hot-pluggable CFP2 form factor
- ✓ 10 channels full-duplex transceiver module
- ✓ Supports 111.8Gb/s aggregate bit rate
- ✓ 10 channels 850nm VCSEL array
- ✓ 10 channels PIN photo-detector array
- ✓ TX input and RX output CDR retiming
- ✓ 8W maximum power dissipation
- ✓ Maximum link length of 300m on OM3 MMF and 400m on OM4 MMF
- ✓ Single MTP/MPO receptacle
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature range: 0 to 70°C
- ✓ Single 3.3V power supply
- ✓ RoHS-6 compliant (lead free)



Applications

- ✓ 100GBASE-SR10 100G Ethernet
- ✓ OTN OTU4 applications

Description

The Gigalight 100GBASE-SR10 & OTU4 400m CFP2 optical transceiver, 100G CFP2 SR10 (GF2-M101-SR10C) is designed for use in 100-Gigabit Ethernet and OTN links up to 400m on Multi-Mode Fiber (MMF). It is compliant with the CFP2 MSA, IEEE 802.3ba 100GBASE-SR4, and OTU4 standards. Digital diagnostics functions are available via an MDIO interface, as specified by the CFP2 MSA. It offers 10 transmit and 10 receive asynchronous channels operating at up to 11.18Gb/s per channel. As shown in Figure 1, the transmitter side of the module consists of a VCSEL array and associated circuitry, which converts 10 parallel electrical data inputs to 10 parallel optical data output signals and also converts 10 parallel optical signals into 10 parallel

electrical signals through an array of PIN photodiodes and associated circuitry. The refclk clock of 161.1328M for 100GE (or 174.6875M for OTU4) is necessary for the CFP2 SR10 module.

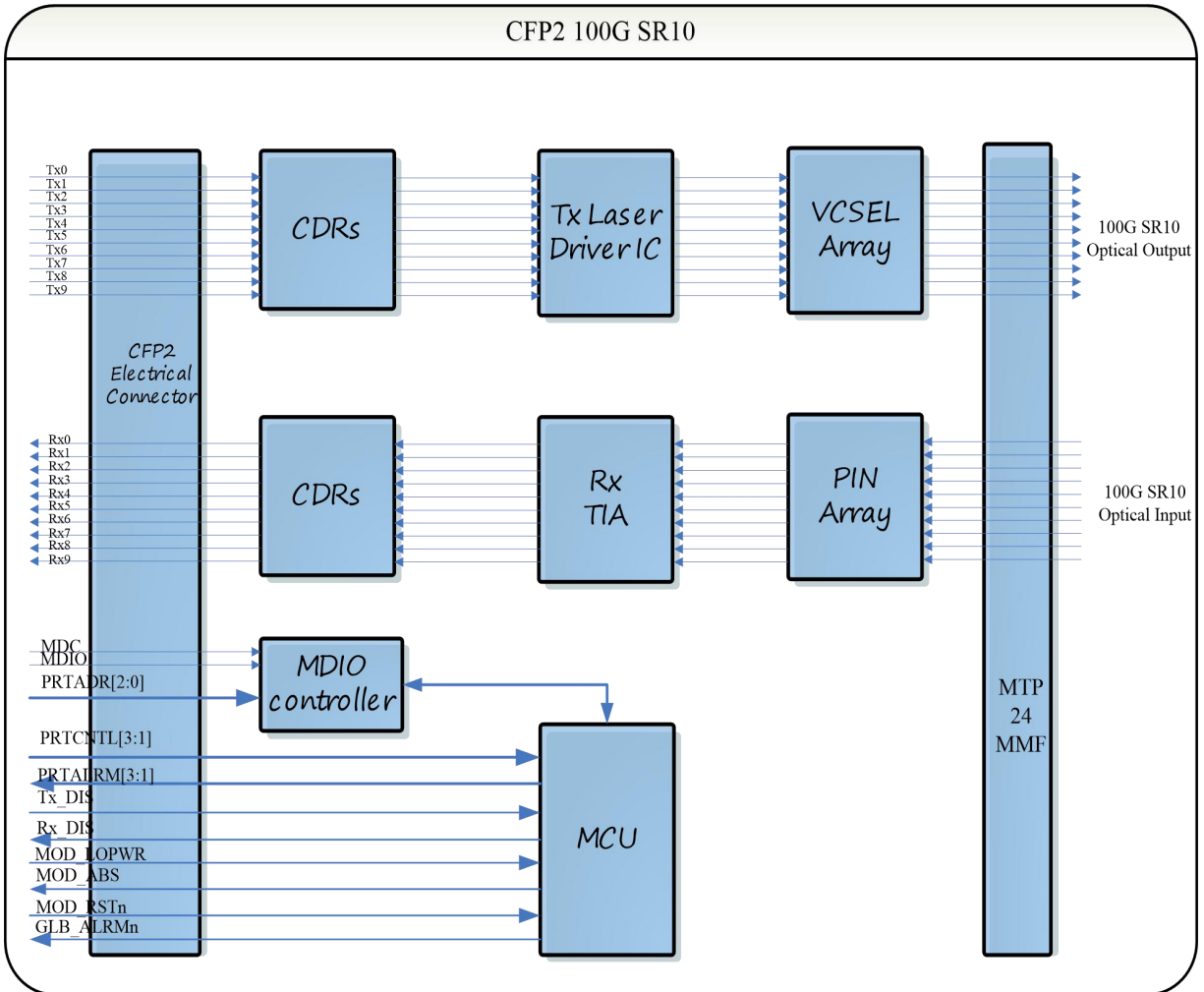


Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.5	3.6	V
Input Voltage	V_{in}	-0.3	$V_{cc}+0.3$	V
Storage Temperature	T_s	-40	85	°C
Case Operating Temperature	T_c	0	70	°C
Humidity (non-condensing)	Rh	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{CC}	3.13	3.3	3.47	V
Operating Case temperature	T_{ca}	0		70	°C
Data Rate Per Lane	fd		10.3125	11.18	Gb/s
Humidity	Rh	5		85	%
Power Dissipation	P_m			8	W
Low Power Mode Dissipation	P_{low}			2	W
Aggregate Bit Rate	BR_{aggr}		103.125	111.8	Gb/s

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential Input Impedance	Z_{in}	90	100	110	ohm	
Differential Output Impedance	Z_{out}	90	100	110	ohm	
Differential Input Voltage Amplitude ¹	ΔV_{in}	120		820	mVp-p	
Differential Output Voltage Amplitude ²	ΔV_{out}	300		820	mVp-p	
Skew	Sw			300	ps	
Bit Error Rate	BER		5E-5			
Input Logic Level High	V_{IH}	2.0		$V_{CC}+0.3$	V	3.3V LVCOMS
		0.84		1.2		1.2V LVCOMS
Input Logic Level Low	V_{IL}	-0.3		0.8	V	3.3V LVCOMS
						0.36
Output Logic Level High	V_{OH}	$V_{CC}-0.2$		V_{CC}	V	3.3V LVCOMS
		1.0		1.5		1.2V LVCOMS
Output Logic Level Low	V_{OL}	0		0.2	V	3.3V LVCOMS
		-0.3				1.2V LVCOMS

Note:

1. Measured between TxnP and TxnN.
2. Measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter (each lane) (T=25°C, V_{CC}=3.3V±5%)						
Center Wavelength	λ_c	840	850	860	nm	
RMS Spectral Width	λ		0.5	0.65	nm	
Average Optical Power	P _{out}	-7.6	-1	2.4	dBm	1
Optical Modulation Amplitude	OMA	-5.6		3	dBm	
Difference in Launch Power between any two lanes(OMA)				4	dB	
Transmitter and Dispersion Penalty	TDP			3.5	dB	
Optical Return Loss Tolerance				12	dB	
Extinction Ratio	ER	3			dB	
Average launch power of OFF transmitter				-30	dB	
Transmitter Eye Mask	Compliant to IEEE802.3ba eye mask specification					
Receiver (each lane) (T=25°C, V_{CC}=3.3V±5%)						
Center Wavelength	λ_c	840	850	860	nm	
RMS Spectral Width	λ		0.5	0.65	nm	
Optical Power Sensitivity	P _{in-min}		-12	-9.9	dBm	2
Optical Power Saturation	P _{in-max}	1			dBm	
Stressed Receiver Sensitivity	P _s			-5.4	dBm	
Optical Return Loss	RI					
Damage Threshold		3.4			dBm	
Optical Modulation Amplitude	OMA			3	dBm	

Note:

1. Measured at the output of the modules optical interface.
2. Measured with BER@10⁻¹² at 10.3125Gb/s per channel.

Pin Description

Part A: Bottom Row Pin Function Definition

Pin	Symbol	Type	I/O	Description
1	GND			
2	TX9n	CML	I	Transmit data input
3	TX9p	CML	I	Transmit data input
4	GND			
5	TX8n	CML	I	Transmit data input
6	TX8p	CML	I	Transmit data input
7	GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A		I/O	Module vendor I/O A.
16	VND_IO_B		I/O	Module vendor I/O B.
17	PRG_CNTL1	LVC MOS w/PU	I	Programmable Control 1 set via MDIO, MSA default: TRXIC_RSTn – TX & RX IC reset. "0" = reset, "1" or NC = enabled or not used
18	PRG_CNTL2	LVC MOS w/PU	I	Programmable Control 2 set via MDIO, MSA default: Hardware Interlock LSB, "00" ≤3W, "01" ≤6W, "10" ≤9W, "11" or NC ≤12W= not used
19	PRG_CNTL3	LVC MOS w/PU	I	Programmable Control 3 set via MDIO, MSA default: Hardware Interlock MSB, "00" ≤3W, "01" ≤6W, "10" ≤9W, "11" or NC ≤12W= not used
20	PRG_ALARM1	LVC MOS	O	Programmable Alarm 1 set via MDIO, MSA default: HIPWR_ON, "1" = Module high power up completed, "0" = Module not high powered up
21	PRG_ALARM2	LVC MOS	O	Programmable Alarm 2 set via MDIO, MSA default: MOD_READY, "1" = ready, "0" = not ready
22	PRG_ALARM3	LVC MOS	O	Programmable Alarm 3 set via MDIO, MSA default: MOD_FAULT, module fault detected, "1" = fault, "0" = no fault
23	GND	GND		
24	TX_DIS	LVC MOS w/PU	I	Transmitter Disable for all channels, "1" or NC = transmitter disabled, "0" = transmitter enabled
25	RX_LOS	LVC MOS	O	Receiver loss of optical signal on any channel, "1" = loss of signal, "0" = normal condition
26	MOD_LOPWR	LVC MOS w/PU	I	Module low power mode. "1" or NC = module in low power (safe) mode, "0" = power-on enabled
27	MOD_ABS	GND	O	Module Absent. "1" or NC = Module absent, "0" = module present. Pull-up resistor on Host
28	MOD_RSTn	LVC MOS w/PD	I	Module Reset. "0" = reset the module, "1" or NC = module enabled, Pull Down resistor in module
29	GLB_ALARMn	LVC MOS	O	Global Alarm. "0" = alarm condition in any MDIO alarm register, "1" = no alarm .Pull-up resistor on Host
30	GND			
31	MDC	1.2V CMOS	I	Management data clock (electrical specs as per IEEE std802.3-2012)
32	MDIO	1.2V CMOS	I/O	Management Data I/O bi-directional data (electrical specs as IEEE std802.3-2012)
33	PRTADR0	1.2V CMOS	I	MDIO port address bit 0
34	PRTADR1	1.2V CMOS	I	MDIO port address bit 1

Optical Transceivers

Data Sheet



Optical Interconnection Design Innovator

35	PRTADR2	1.2V CMOS	I	MDIO port address bit 2
36	VND_IO_C		I/O	Module vendor I/O C.
37	VND_IO_D		I/O	Module vendor I/O D.
38	VND_IO_E		I/O	Module vendor I/O E.
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			3.3V Module power Supply
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
46	GND			
47	RX9n	CML	O	Received data output
48	RX9p	CML	O	Received data output
49	GND			
50	RX8n	CML	O	Received data output
51	RX8p	CML	O	Received data output
52	GND			

Part B: Top Row Pin Function Definition

Pin	Symbol		Pin	Symbol
104	GND		78	REFCLKp
103	TX7n		77	GND
102	TX7p		76	RX7n
101	GND		75	RX7p
100	TX6n		74	GND
99	TX6p		73	RX6n
98	GND		72	RX6p
97	TX5n		71	GND
96	TX5p		70	RX5n
95	GND		69	RX5p
94	TX4n		68	GND
93	TX4p		67	RX4n
92	GND		66	RX4p
91	TX3n		65	GND
90	TX3p		64	RX3n
89	GND		63	RX3p
88	TX2n		62	GND
87	TX2p		61	RX2n
86	GND		60	RX2p
85	TX1n		59	GND
84	TX1p		58	RX1n
83	GND		57	RX1p
82	TX0n		56	GND
81	TX0p		55	RX0n
80	GND		54	RX0p
79	REFCLKn		53	GND

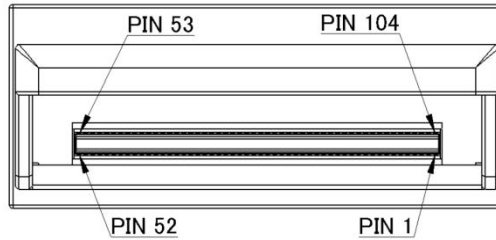


Figure 2. Pad Layout of the CFP2 module

CFP2 Optical Interface Lanes and Assignment

Figure 3 shows the orientation of the multimode fiber facets of the optical connector.

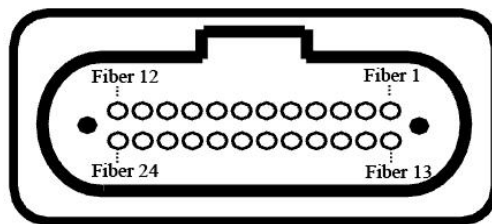


Figure 3. Outside view of the CFP2 module MPO receptacle

Lane Assignment

Fiber	Symbol	Corresponding Electrical pins	Fiber	Symbol	Corresponding Electrical pins
1	Unused		13	Unused	
2	RX0	54, 55	14	TX0	81, 82
3	RX1	57, 58	15	TX1	84, 85
4	RX2	60, 61	16	TX2	87, 88
5	RX3	63, 64	17	TX3	90, 91
6	RX4	66, 67	18	TX4	93, 94
7	RX5	69, 70	19	TX5	96, 97
8	RX6	72, 73	20	TX6	99, 100
9	RX7	75, 76	21	TX7	102, 103
10	RX8	50, 51	22	TX8	5, 6
11	RX9	47, 48	23	TX9	2, 3
12	Unused		24	Unused	

Mechanical Dimensions

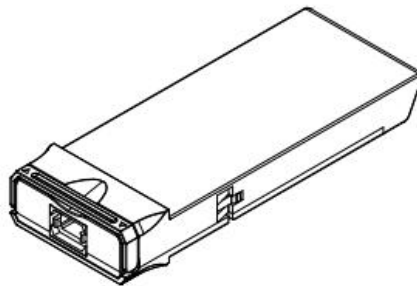
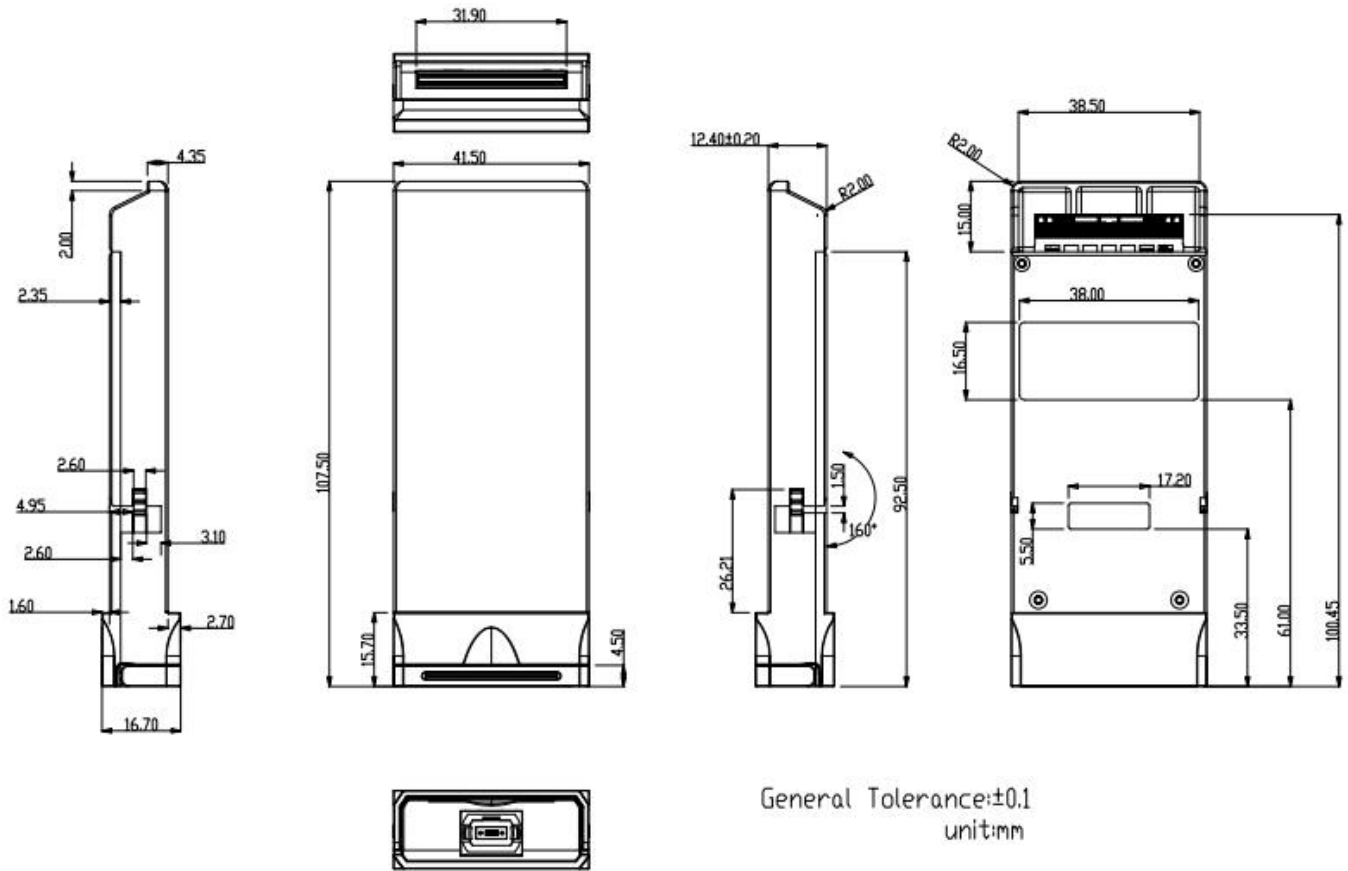


Figure 4. Mechanical Specifications

Ordering Information

Product Description	Part Number
CFP2 SR10, 111.8Gb/s, 850nm, 400m, MMF, MTP/MPO	GF2-M101-SR10C

References

1. CFP2 MSA
2. Ethernet 100GBASE-SR10
3. OTN OTU4

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

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Revision History

Revision	Level	Date	Description
V0	Preliminary	Aug 2016	Advance Release.