

25GBASE-LR 10km SFP28 Optical Transceiver GSS-SP0250-LRC

Features

- ✓ Hot-pluggable SFP28 form factor
- ✓ Supports 25.78125Gb/s data rate
- ✓ 1310nm DFB laser and PIN photo-detector
- ✓ Internal CDR on both transmitter and receiver channel
- ✓ 1.5W maximum power dissipation
- ✓ Maximum link length of 10km on SMF
- ✓ Duplex LC receptacle
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature range: 0 to 70°C
- ✓ Single 3.3V power supply
- ✓ RoHS-6 compliant (lead free)



Applications

- ✓ 25GBASE-LR Ethernet

Description

The Gigalight 25GBASE-LR 10km SFP28 optical transceiver (GSS-SPO250-LRC) is designed for use in 25-Gigabit Ethernet links up to 10km on Single Mode Fiber (SMF). It is compliant to IEEE802.3by 25GBASE-LR, SFF-8472 Rev 12.1 and compatible with SFF-8432 and applicable portions of SFF-8431. The electrical interface uses a 20 contact edge type connector. This module incorporates Gigalight proven circuit and technology to provide reliable long life, high performance, and consistent service.

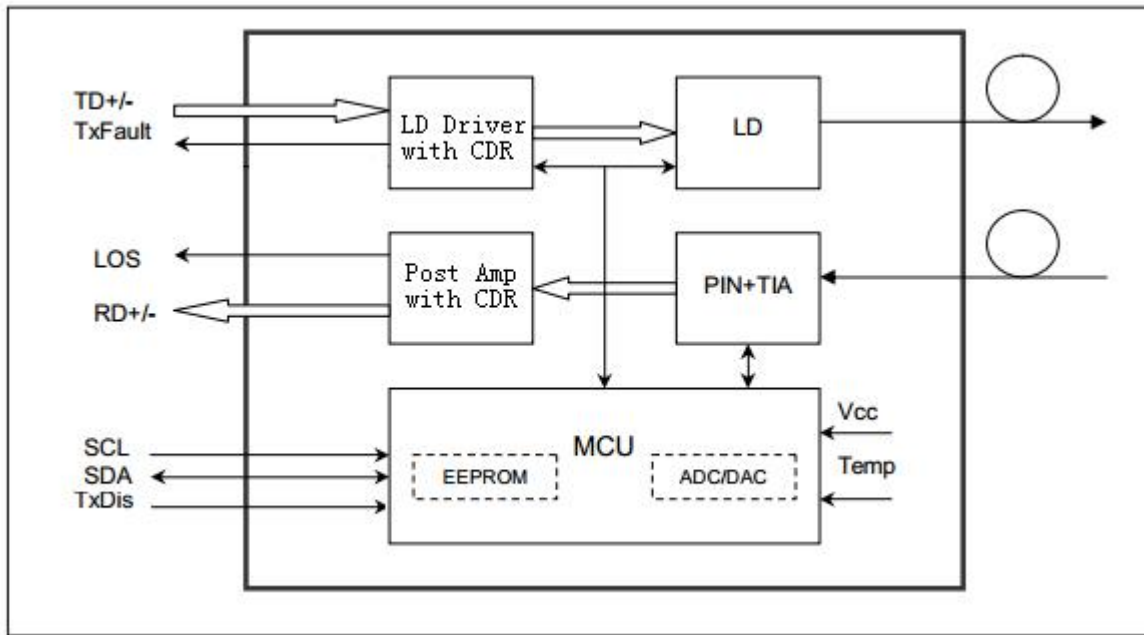


Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	0	3.6	V
Storage Temperature	T_s	-40	85	°C
Operating Humidity		5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	T_c	0		70	°C
Power Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Power Supply Current	I_{cc}			450	mA

Optical and Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Data Rate ¹	BR			25.78125	Gb/s
Center Wavelength	λ_c	1290	1310	1330	nm
Spectral Width (-20dB)	σ			1	nm
Side Mode Suppression Ratio	SMSR	30			dB
Average Output Power	P_{avg}	-1		4	dBm
Extinction Ratio	ER	4.0			dB
Differential Data Input Swing	$V_{IN,PP}$	180		700	mV
Input Differential Impedance	Z_{IN}	90	100	110	Ω
TX Disable	Disable	2.0		V_{cc}	V
	Enable	0		0.8	V

TX Fault	Fault		2.0		V _{cc}	V
	Normal		0		0.8	V
Receiver²						
Receiver Sensitivity (OMA)	P _{sens}			-11.5		dBm
Stressed Sensitivity (OMA)				-6.8	-11.2	dBm
Average Receiver Power	Rx _{max}				2	dBm
LOS De-Assert	LOS _D				-12	dBm
LOS Assert	LOS _A				-13	dBm
LOS Hysteresis	LOS _H	0.5				dB
Differential data output swing	V _{out,PP}	300			900	mV
LOS	High	2.0			V _{cc}	V
	Low				0.8	V

Parameter	Symbol	Min.	Max.	Unit	Conditions
Tx_Disable assert time	t _{off}		100	μs	Rising edge of Tx_Disable to fall of output signal below 10% of nominal
Tx_Disable negate time	t _{on}		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t _{2w_start_up}		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t _{start_up}		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t _{start_up_cooled}		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t _{power_level2}		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t _{power_down}		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements
Tx_Fault assert	Tx_Fault_on		1	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault assert for cooled module	Tx_Fault_on_cooled		50	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault Reset	t _{reset}	10		μs	Time Tx_Disable must be held high to reset Tx_Fault
RS0, RS1 rate select timing for FC	t _{RS0_FC} , t _{RS1_FC}		500	μs	From assertion till stable output
RS0, RS1 rate select timing non FC	t _{RS0} , t _{RS1}		24	ms	From assertion till stable output
Rx_LOS assert delay	t _{los_on}		100	μs	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t _{los_off}		100	μs	From occurrence of presence of signal to negation of Rx_LOS

Figure 2. Timing and Electrical

Diagnostics Specification

Parameter	Range	Unit	Accuracy	Calibration
Temperature	0 to 70	°C	±3°C	Internal / External
Voltage	3.0 to 3.6	V	±3%	Internal / External
Bias Current	0 to 100	mA	±10%	Internal / External
TX Power	-1.5 to 4.5	dBm	±3dB	Internal / External
RX Power	-14 to 4.5	dBm	±3dB	Internal / External

Digital Diagnostic Memory Map

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA). The diagnostic information with internal calibration or external calibration all are implemented, including received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring. The digital diagnostic memory map specific data field defines as following.

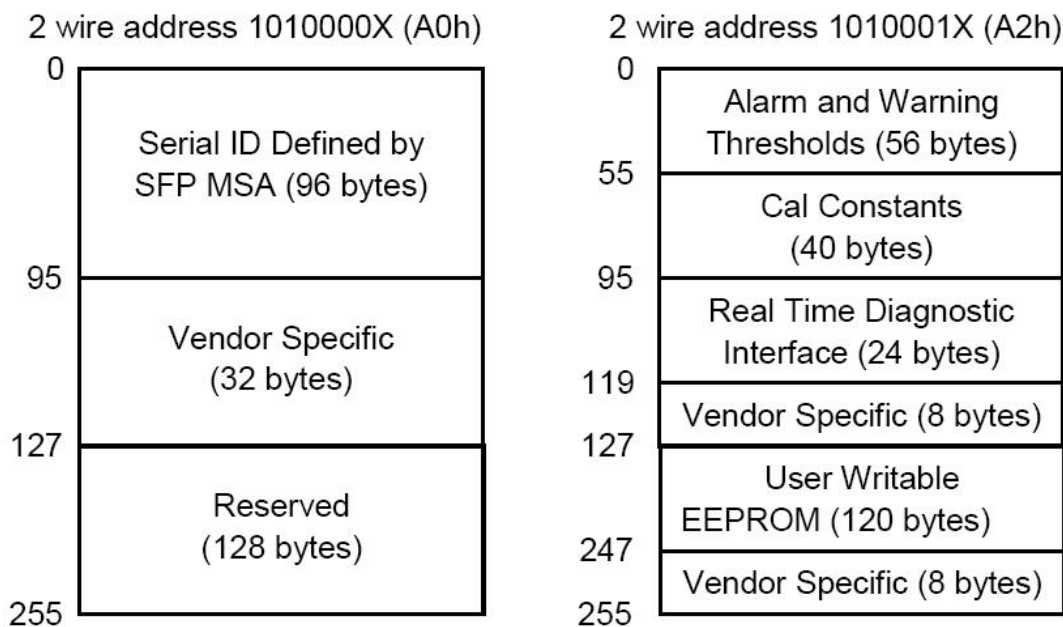


Figure 3. Digital Diagnostic Memory Map

Pin Definitions

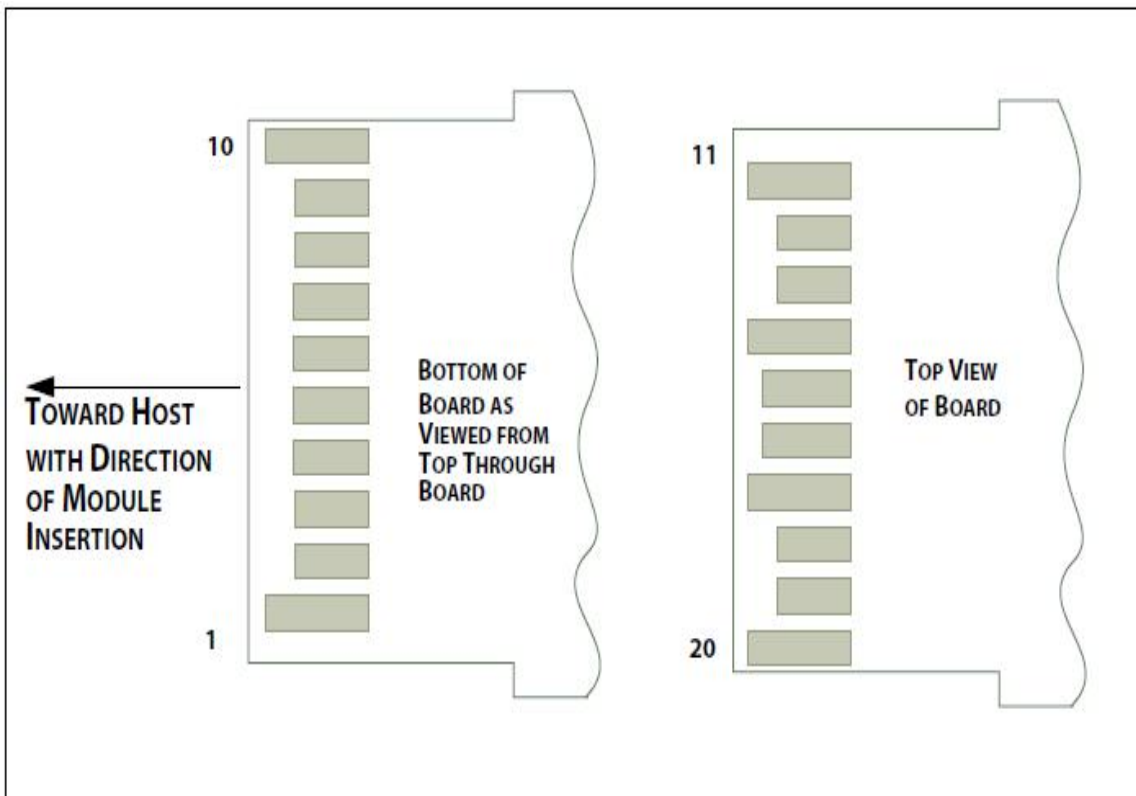
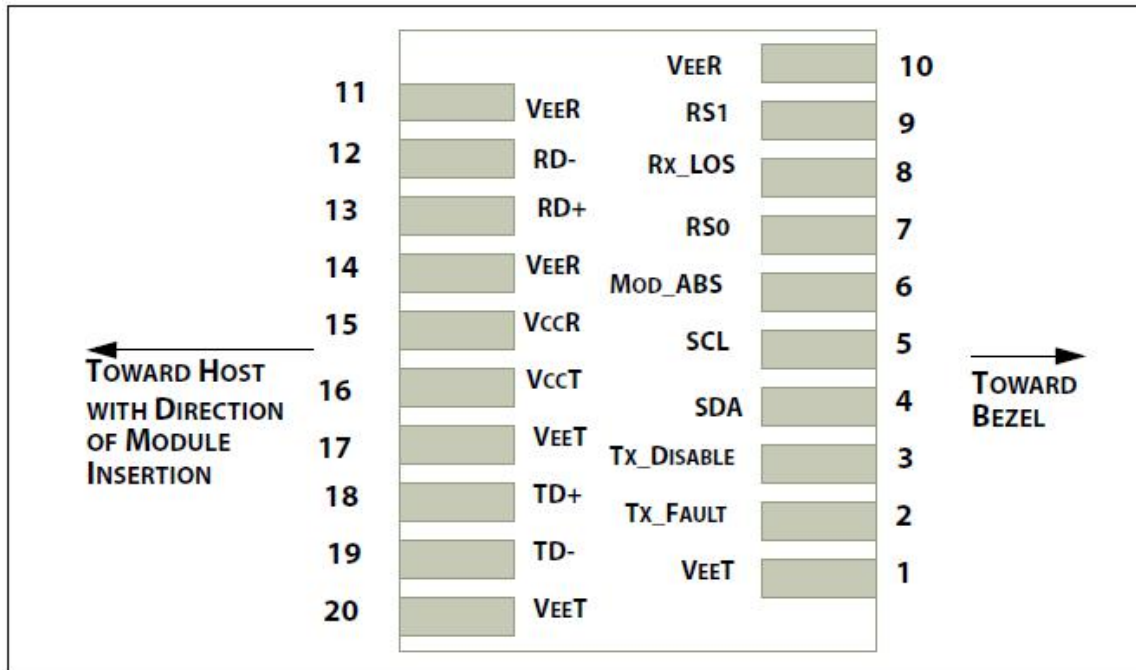


Figure 4. Pin Definition

Pin Description

Pin	Logic	Symbol	Name/Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser output	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	2
6		MOD_ABS	Module Definition, Grounded in the module	
7	LVTTL-I	RS0	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTL-I	RS1	Transmitter Rate Select (not used)	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

Notes:

1. Module ground pins GND are isolated from the module case.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

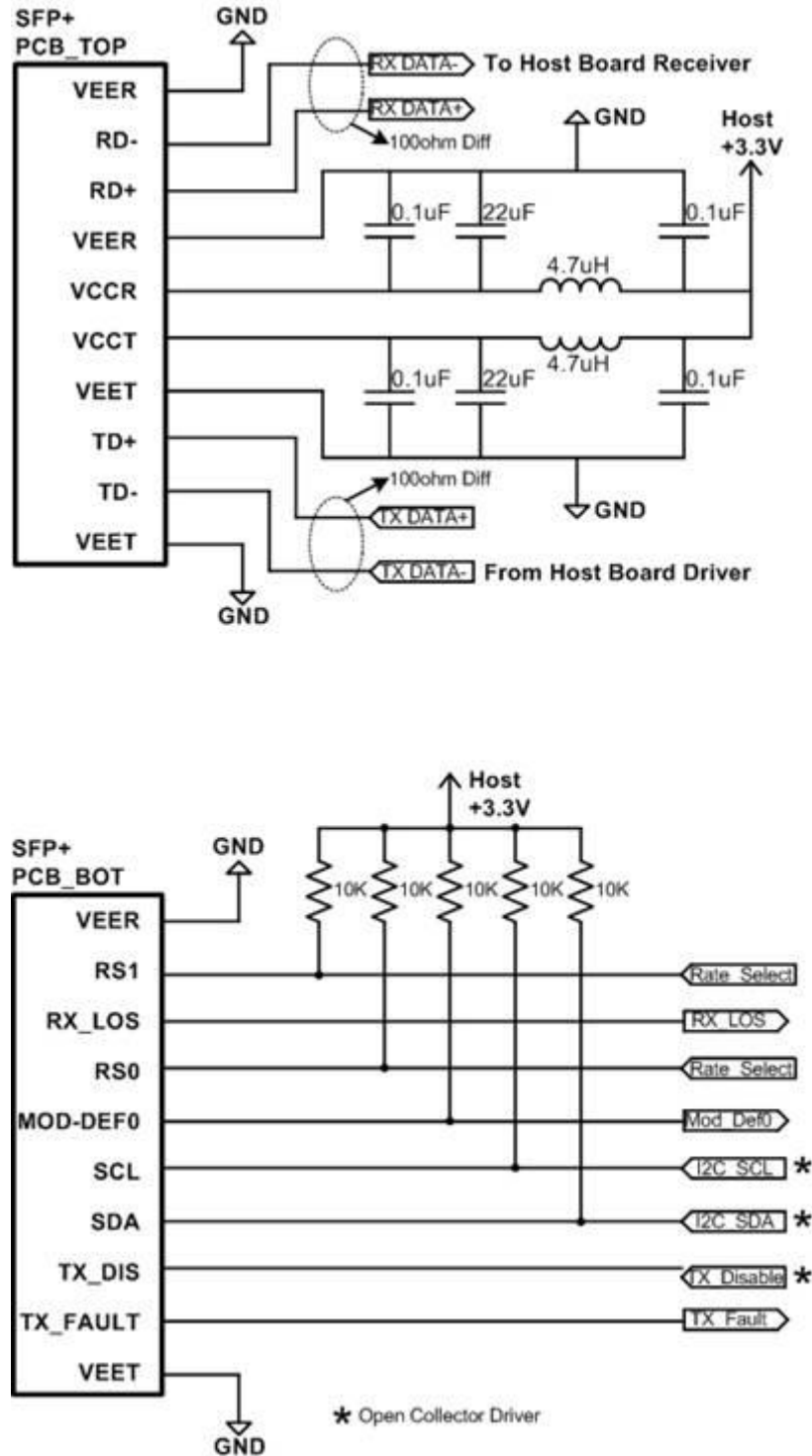


Figure 5. Recommended Interface Circuit

Mechanical Dimensions

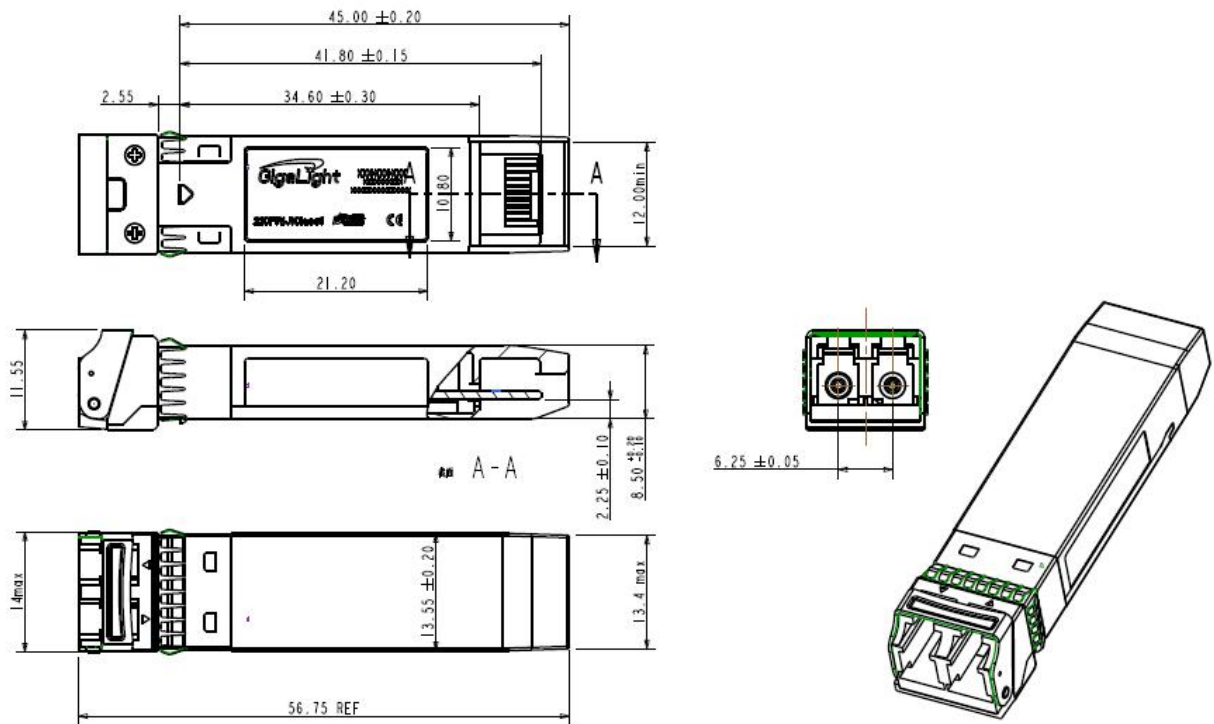


Figure 6. Mechanical Specifications

Ordering Information

Product Description	Part Number
SFP28 LR, 25.78125Gb/s, 1310nm, 10km, SMF, LC	GSS-SP0250-LRC

Important Notice

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Optical Transceivers Data Sheet



Optical Interconnection Design Innovator

E-mail: sales@gigalight.com

Official Site: www.gigalight.com

Revision History

Revision	Level	Date	Description
V0	Preliminary	Jan 2015	Advance Release.