100G CFP2 ER4 40km Optical Transceiver
GF2-S101-ER4C

Features

- 4 channels full-duplex transceiver module
- Transmission data rate up to 28Gb/s per channel
- 4 LAN-WDM EML Integrated TOSA Cooling transmitter
- 4 channels PIN-base Integrated ROSA with SOA
- Compliant with CFP2 hardware specification
- Compliant with CFP MSA management specification
- Compliant to IEEE 802.3ba specification for 100GBASE-ER4
- Compliant to OTU4
- Transmission distance up to 40km on SMF
- 4 parallel electrical serial interface and AC coupling of CML signals
- MDIO real-time digital diagnostic and control capabilities
- Internal CDR circuits on both receiver and transmitter channels
- Hot pluggable
- Total Power Consumption <9W
- Operating case temperature 0°C to +70°C
- 3.3V power supply
- Duplex LC receptacle optical interface
- RoHS 6 compliant (lead free)

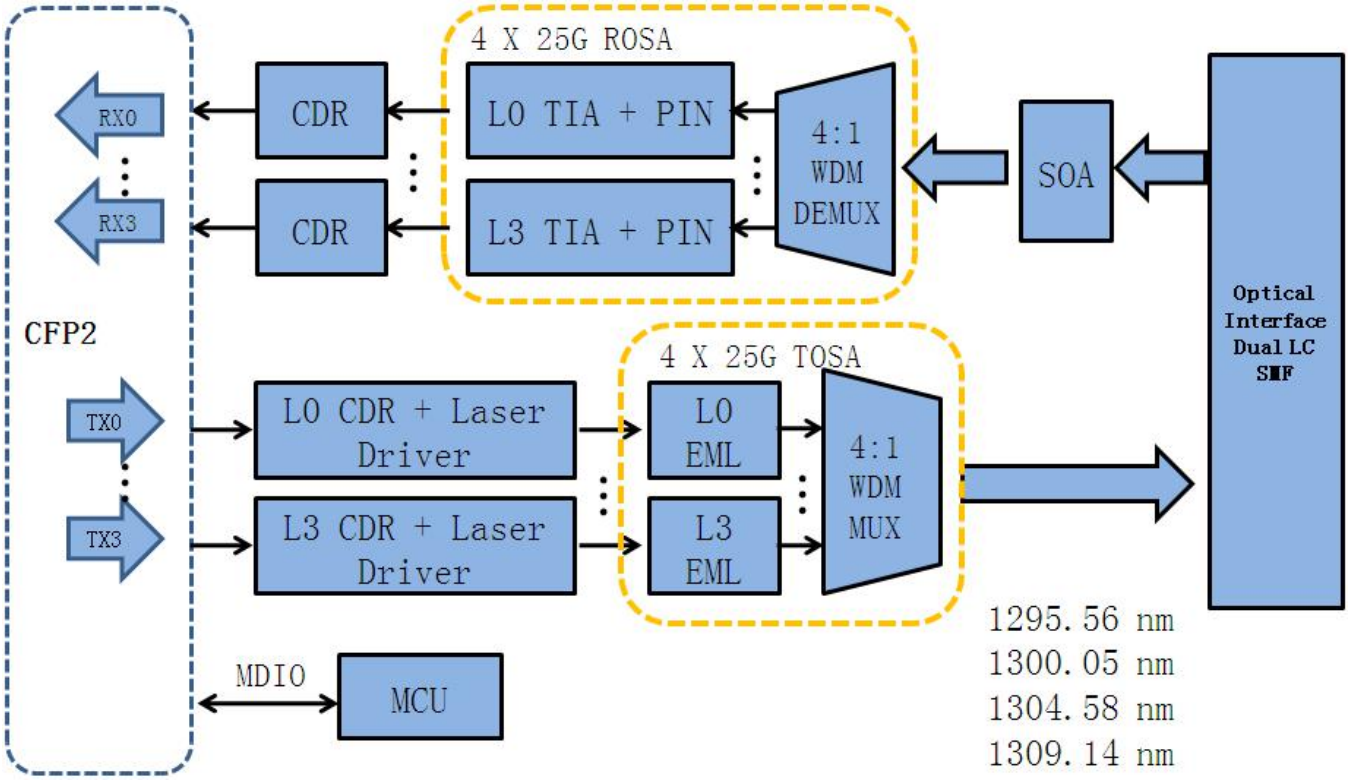
Applications

- 100GbE IEEE 802.3ba 100GBASE-ER4
- ITU-T G.959.1 OTU4 (4L1-9C1F)
- Switch to switch interface or Switch to router interface

Description

The Gigalight 100G CFP2 ER4 optical transceiver is a hot pluggable small form-factor transceiver module. It is designed for use in 100G Ethernet links and 4x28G OTN client interfaces over single mode fiber. It is

compliant with the CFP MSA, IEEE 802.3ba 100GBASE ER4 and OTU4 4L1-9C1F. Digital diagnostics functions are available via the MDIO interface. The module converts 4 input channels of 25Gb/s electrical data to 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission. On the receiver side, a 100Gb/s optical input into SOA, and then the module de-multiplexes the 100Gb/s optical into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data. The module is a multi-rate optical transceiver which data rate up to 28Gb/s per channel. The high performance cooled LAN WDM EML Integrated TOSA and PIN-base Integrated ROSA with SOA provide superior performance for Telecom and Datacom applications up to 40km links.



100GE CFP2 ER4 Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Supply Voltage	VCC	V	-0.5	3.6
Storage Temperature	Ts	℃	-40	85
Operating Case Temperature	Tc	℃	0	70
Relative Humidity (Non condensation)	-	%	5	85

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature	Tc	℃	0	-	70
Supply Voltage	VCC	V	3.13	3.3	3.47
Supply Current	ICC	A	-	-	2.8
Power Dissipation	-	W	-	-	9

Optical Characteristics

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Value			Notes
			Min	Typ	Max	
Optical Transmitter Characteristics						
Signaling Rate for Each Lane (100GbE)	-	Gbps		25.78125		
Signaling Rate for Each Lane (OTU4)				27.9525		
Four lane Wavelength Range	入 1	nm	1294.53	1295.56	1296.59	
	入 2		1299.02	1300.05	1301.09	
	入 3		1303.54	1304.58	1305.63	
	入 4		1308.09	1309.14	1310.19	
Side Mode Suppression Ratio	SMSR	dB	30			
Total Average Launch		dBm			8.9	
Average Launch Power for Each Lane(100GbE)	Pa	dBm	-2.9		+2.9	
Average Launch Power for Each Lane(OTU4)			-2.7		+2.9	
Difference in launch power between any two lanes (Average and OMA)		dB			3.6	
Extinction Ratio	ER	dB	8			

Average Launch Power OFF	Poff	dBm			-30	
Optical Return Loss Tolerance	dB				20	
Optical Receiver Characteristics						
Receiver Sensitivity in OMA for Each Lane(100GbE)	Pmin	dBm	-	-	-21.4	1
Equivalent Sensitivity for Each Lane(OTU4)					-23.2	
Los Assert		dBm	-35		-26	
Los De-assert		dBm			-25	
Los Hysteresis		dBm	0.5			
Damage Threshold, each Lane	THd	dBm	5.5			2
Receive Power In OMA for Each Lane	PinOMA	dBm			4.5	
Difference in Receive Power between any Two Lanes (Average and OMA)	Prx,diff	dB			4.5	
Average Receive Power for Each Lane(100GbE)	Pin	dBm	-20.9		4.5	
Average Receive Power for Each Lane(OTU4)			-20.7		4.5	

Note:

1. Minimum average optical power measured at BER less than 1E-12, with a 2^{31}-1 PRBS.
2. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

Electrical Characteristics

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Note
Differential Data Output Swing	Vout,pp	mV	300	-	850	
Differential Input Voltage Swing	Vin,pp	mV			900	
Differential Signal Output Resistance		Ω	90	-	110	
Differential Signal Input Resistance		Ω	90	-	110	

Low Speed Electrical Interface

Parameter	Symbol	Unit	Min	Max	Note
Input Voltage	V_{IH}	V	2.0	V_{cc3} + 0.3	1

	V_{IL}	V	-0.3	0.8	
Output Voltage	V_{OH}	V	V_{dd3}-0.5	V_{dd3} + 0.3	
	V_{OL}	V	0.0	0.4	
Input Leakage Current	3.3VIL	uA	-10	10	
Minimum Pulse Width of Control Pin Signal	T_CNTL	us	100		
1.2V LVCMOS Electrical Characteristics					
Input High Voltage	1.2VIH	V	0.84	1.5	
Input Low Voltage	1.2VIL	V	-0.3	0.36	
Input Leakage Current	1.2IIN	uA	-100	+ 100	
Output High Voltage	1.2VOH	V	1.0	1.5	
Output Low Voltage	1.2VOL	V	-0.3	0.2	
Output High Current	1.2IOH	mA		-4	
Output Low Current	1.2IOL	mA	+4		
Input Capacitance	Ci	pF		10	

Note1: Vdd3 is host +3.3V power supply.

Hardware Control Pins

The CFP2 Module support real-time control functions via hardware pins, listed in the following table:

Hardware Control Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
17	PRG_CNTL1	Programmable Control 1 MSA Default:TRXIC_RSTn , TX&RX ICs reset, “0”:reset;”1”	I	3.3V LVCMOS	per CFP MSA Management Interface Specification		Pull-Up Note1
18	PRG_CNTL2	Programmable Control 2 MSA Default : Hardware Interlock LSB	I	3.3V LVCMOS			Pull-Up Note1
19	PRG_CNTL3	Programmable Control 3 MSA Default:Hardware Interlock MSB	I	3.3V LVCMOS			Pull-Up Note1
26	M0D_L0PWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up Note1
28	M0D_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2
24	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up Note1

Note1: Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP2 module Note2: PuH-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP2 module

Hardware Alarm Pins

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
20	PRG_ALRM1	Programmable Alarm 1 MSA Default:HIPWR_0N	O	3.3V LVCMOS			
21	PRG_ALRM3	Programmable Alarm 3 MSA Default: MOD_FAULT	O	3.3V LVCMOS			
22	MOD_ABS	Module Absent	O	3.3V LVCMOS			
27	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Absent	Present	Pull-Down Note1
25	PRG_ALRM3	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note1: Pull-Down resistor (<100ohm) is located within the CFP module. Pull-up should be located on the host

Management Interface Pins(MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. The CFP MDIO pins are listed in

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
29	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
32	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
31	MDC	MDIO Clock	I	1.2V LVCMOS			
33	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
34	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
35	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

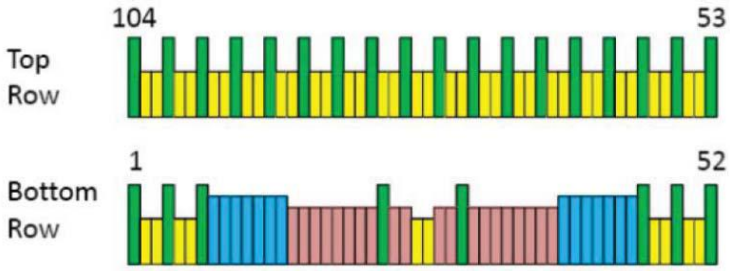
Timing Parameters for CFP2 hardware Signal Pins are listed in the following table.

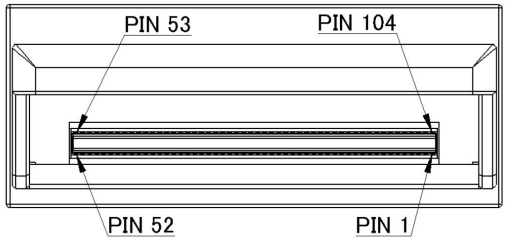
Parameter	Symbol	Min	Max	Unit	Notes&Conditions

Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific May depend on current state Condition when signal is applied .See Vendor Datasheet
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			ms	Value is dependent upon module start-up time.Please See register〃Maximum High-Power-up ime〃in “CFP MSA Management Interface Specification”
Receiver Loss of Signal Assert Time	t_loss_assert		100	us	Maximum value designed to support telecom applications
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	us	Maximum value designed to support telecom applications
Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	ms	This is a logical “OR” of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical “OR” of Associated MDIO alarm& status registers.Please see MDIO document for further details
Management Interface Clock Period	t_prd	250	10000	ns	MDC is 4MHz rate(Max)
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific
Transmitter Enabled(TX_DIS_asserted)	t_assert		100	ms	Value is dependent upon module start-up time.Please See register “Maximum TX-Turn-on Time” in “CFP MSA Management Interface

Optional Transmitter and Receiver Monitor Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency			3220		MHz	1/8 of Network lane rate
Output Differential Voltage	VDIFF	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	





Pad Layout of the CFP2 module

PIN#	Name	I/O	Logic	Description
1	GND			
2	(TX_MCLKn)	O	CML	For optical waveform testing. Not for normal use
3	(TX_MCLKp)	O	CML	For optical waveform testing. Not for normal use
4	GND			
5	N.C.			
6	N.C.			
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate, or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			

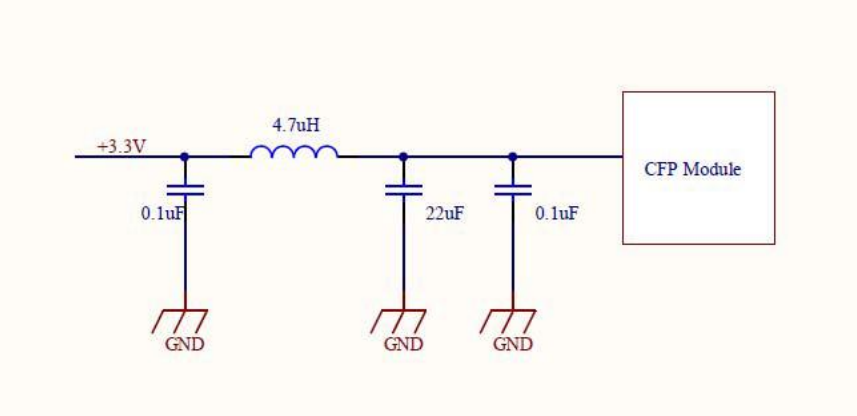
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect!
16	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect!
17	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
18	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
19	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO
23	GND			
24	TX_DIS	I	LVCMOS	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0"= transmitter enabled
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O		Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 1
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 2
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 3
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			

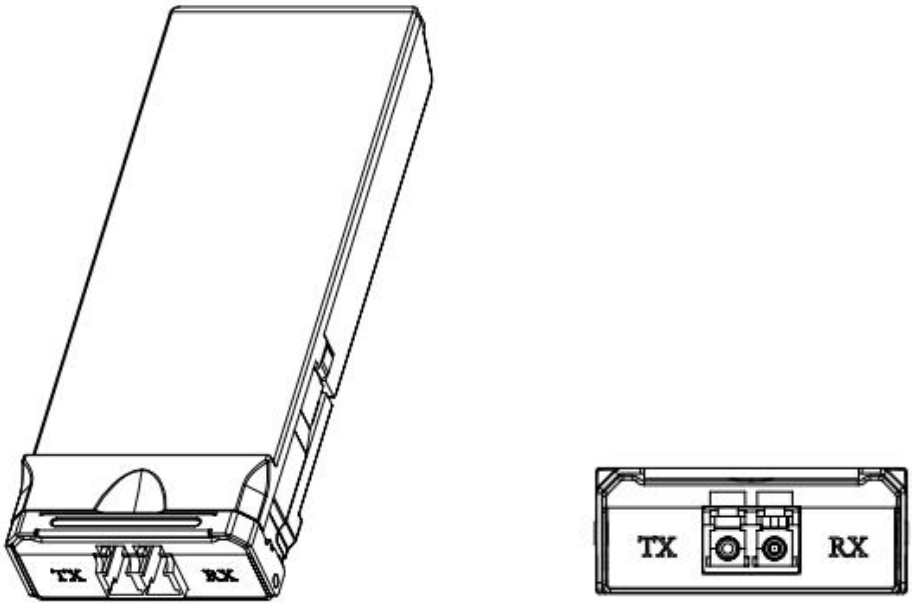
40	3.3V_GND			
41	3.3V			
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 1
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 2
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 3
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
46	3.3V_GND			
47	N.C.			
48	N.C.			
49	GND			
50	(RX_MCLKn)	O	CML	For optical waveform testing. Not for normal use.
51	(RX_MCLKp)	O	CML	For optical waveform testing. Not for normal use.
52	GND			
53	GND			
54	N.C.			
55	N.C.			
56	GND			
57	RXOp	O	CML	Output Data
58	RXOn	O	CML	Inverted Output Data
59	GND			
60	RX1p	O	CML	Output Data
61	RX1n	O	CML	Inverted Output Data

62	GND			
63	N.C.			
64	N.C.			
65	GND			
59	GND			
60	RX1p	O	CML	Output Data
61	RX1n	O	CML	Inverted Output Data
62	GND			
63	N.C.			
64	N.C.			
65	GND			
70	RX2n	O	CML	Inverted Output Data
71	GND			
72	RX3p	O	CML	Output Data
73	RX3n	O	CML	Inverted Output Data
74	GND			
75	N.C.			
76	N.C.			
77	GND			
78	NC			
79	NC			
80	GND			
81	N.C.			
82	N.C.			
83	GND			
84	TXOp	I	CML	Input Data
85	TXOn	I	CML	Inverted Input Data
86	GND			
87	TX1p	I	CML	Input Data
88	TX1n	I	CML	Inverted Input Data
89	GND			
90	N.C.			
91	N.C.			
92	GND			
93	N.C.			
94	N.C.			
95	GND			
96	TX2p	I	CML	Input Data
97	TX2n	I	CML	Inverted Input Data

98	GND			
99	TX3p	I	CML	Input Data
100	TX3n	I	CML	Inverted Input Data
101	GND			
102	N.C.			
103	N.C.			
104	GND			

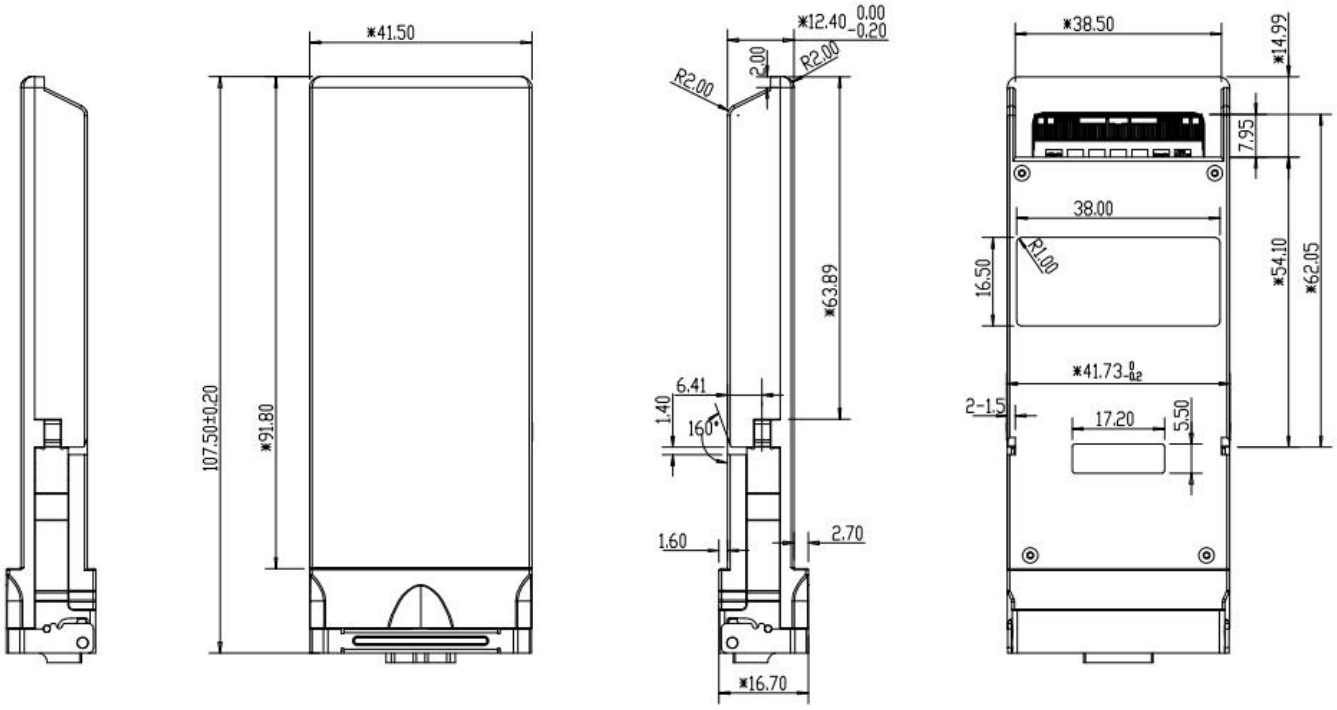
Typical Application Circuit for Power Supply





Unit(MM),General Tolerance:±0.1mm

Mechanical Dimensions



Ordering information

Part Number	Product Description
GF2-S101-ER4C	CFP2, LAN-WDM EML transmitter, PIN-base Integrated ROSA with SOA ,100GE/OTU4,40km

Regulatory Compliance

Feature	Standard
Laser Safety	IEC 60825-1:2014 (Third Edition)
Environmental protection	2011/65/EU
CE EMC	EN55032：2015 EN55024：2010+A1：2015 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014

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